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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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EXAMINER	
JORGENSEN, LELAND R	

ART UNIT	PAPER NUMBER
2675	

DATE MAILED: 06/29/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/986,707	LEE ET AL.	
	Examiner	Art Unit	
	Leland R. Jorgensen	2675	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1 - 38* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1 - 38* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Objections

1. In view of applicants amendment filed 24 November 2004, the informality objection to Claim 22 is withdrawn.

Claim Rejections - 35 USC § 102

2. The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

3. Claims 1, 7 – 15, and 21 - 28 are rejected under 35 U.S.C. 102(e) as being anticipated by Nakamura et al, USPN 6,069,620.

Claims 1 and 15

Nakamura teaches a liquid crystal display device comprising a control unit [control section 26] for receiving a RGB picture signal [data signal] and a first timing signal [sync signal] from the external and outputting the RGB picture signal a second timing signal for displaying the RGB picture signal on a screen. Nakamura, col. 4, lines 15 – 23; and figures 1 – 4. Nakamura teaches a gate driver [gate line driving circuit 16] for outputting a scan signal, a source driver [data line driving circuit 16] for a picture signal; and an LCD panel including a plurality of gates lines [8] for transmitting the scan signal, a plurality of source line [data lines 6] intersecting the plurality of gate lines for transmitting the image signal, a plurality of switching elements [TFT 10] connected to the plurality of gate line and source line, respectively, and a plurality of picture

electrodes [not shown but described in Nakamura, col. 3, line 67 – col. 4, line 4] connected to the plurality of switching element for responding operation of the plurality of switching element, arranged in a matrix type. Nakamura, col. 3, line 57 – col. 4, line 24; and figure 1. Nakamura teaches that fast transition into a bend state is induced by an application of a bias voltage at initial operation. Nakamura, col. 2, line 33 – 42; col. 4, lines 47 – 57; and figure 2. Nakamura teaches a power saving mode for backlight. Nakamura, col. 7, line 47 – 64. It is inherent that such system include a backlight control signal, a first direct current power conversion unit responsive to an ON state of the backlight control signal for applying a backlight driving voltage; and a backlight unit for outputting light according to the application of the backlight driving to voltage.

Nakamura teaches a common electrode line. Nakamura, col. 3, line 67 – col. 4, line 4. Nakamura teaches that the common electrode line [common electrode] receives the bias voltage [10V-30V] at an initial operation [period t1 when the power-on reset signal is output for t1 seconds] of the LCD. Nakamura, col. 6, lines 34 – 43; and figure 7. In the embodiment shown in figure 7, the voltage is applied to both the common electrode and the storage capacitance electrode. Nakamura teaches, however, that the bias voltage may be applied exclusively to the common electrode.

> Although in this embodiment voltages are applied to both of the common electrode and the storage capacitance lines, a modification is possible in which a voltage is applied to one of those, for instance, the common electrode but no voltages are applied to the storage capacitance lines.

Nakamura, col. 7, lines 1 – 5.

Claims 7 and 21

Nakamura teaches that the control unit comprises a switching unit [switch circuit 44] for performing a first switching of at least one of a gate voltage [Vg] for the scan signal and a data voltage [Vd] for the picture signal, and performing a second switching of at least one of a bias voltage [Vcs] and a common electrode voltage [Vcom] for outputting the bias voltage. Nakamura, col. 6, lines 15 – 25; and figure 6. Nakamura teaches a timing controller [power-on signal circuit 48 with startup re-orientation controller 46] for outputting a first switching signal to control the first switching to the switching unit and outputting a second switching signal to control the second switching to the switching unit so that fast transition into bend state of the liquid crystal arranged in the LCD panel is accomplished. Nakamura, col. 6, lines 26 – 42; and figures 6 & 7.

Claims 8 and 22

Nakamura teaches a second direct current power conversion unit for outputting the bias voltage to the switching unit. Nakamura, col. 7, lines 11 – 25; and figures 1, 6, and 8.

Claims 9, 12, 23, and 26

Nakamura teaches that the switching unit comprises a first switching unit [top switch shown in switch circuit 44] for ON/OFF switching the gate voltage, the data voltage, and the backlight driving voltage according to the first switching signal; and a second switching unit [bottom switch shown in switch circuit 44] for ON/OFF switching the bias voltage and the common electrode voltage according to the second switching signal. Nakamura, col. 6, lines 15 – 42; and figures 6 & 7.

Claims 10, 13, 24, and 27

Nakamura teaches that the timing controller controls output of the gate voltage, the data voltage, the bias voltage, and the common electrode voltage at initial operation, when a first period elapses, interrupts output of the gate voltage, the data voltage, and the common electrode voltage and controls a selection of the bias voltage, when a second period elapses, controls a selection of the common electrode voltage, and when a third period elapses, controls output of the gate voltage, the data voltage, and the backlight driving voltage and controls a selection of the common electrode voltage. Nakamura, col. 6, line 34 – col. 7, line 5; and figure 7.

Claims 11, 14, 25, and 28

Nakamura teaches that the timing controller controls an alternative selection of a high voltage and a low voltage when the selection of the bias voltage is controlled. Nakamura, col. 6, line 34 – col. 7, line 5; and figure 7.

Claim Rejections - 35 USC § 103

4. Claims 2 - 6, 16 – 20, and 29 – 38 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura et al. in view of Hattori et al., USPN 6,476,792 B2.

Claims 2 and 16

Nakamura teaches a control unit. Nakamura does not specifically teach a timing controller for the backlight.

Hattori teaches a control unit [11] that comprises a timing controller [backlight driving circuit 14] for outputting a first switching signal the backlight control signal of OFF state at initial operation and outputting a second switching signal and the backlight control signal of ON

state after a predetermined period elapses. Hattori, col. 11, lines 9 – 14; and figure 3. A second direct current power conversion unit [transition-driving circuit 13] outputs a predetermined bias voltage. Hattori, col. 11, lines 15 – 20. A switching unit [switch 15] outputs the bias voltage as the bias signal when the first switching signal is applied by the timing controller and the common electrode voltage as bias signal when the second switching signal is applied by the timing controller. Hattori, col. 11, lines 26 – 42; and figure 3.

It would have been obvious to one of ordinary skill in the art at the time of the invention to combine the backlight timing controller as taught by Hattori with the liquid crystal display device as taught by Nakamura to conserve power that would be consumed by the backlight during the start up period. Hattori invite such combination by teaching,

> Generally, a backlight is turned on when a main power of the apparatus is switched on. In liquid crystal televisions, an output of voice from a speaker starts simultaneously. However, in liquid crystal display apparatuses for carrying out the transition of the alignment of liquid crystal molecules in the liquid crystal layer to a predetermined alignment in advance of displaying, it occasionally takes a long time to be shifted to the ordinary display- driving mode. It is a waste of energy to switch on the backlight for the shift period to the display-driving mode or the transition period. The display having many point alignment defects and plane alignment defects due to pixels with no transition or under transition as well as the blinking of the whole screen due to the application of the voltage pulse for transition are the causes of users' discomfort and anxiety. Disappearance of the above-mentioned defects due to alignment transition can delete such sense of incongruity thereby realizing liquid crystal display apparatuses which can display images with high quality and are excellent in commercial view.

Hattori, col. 2, line 52 – col. 3, line 3.

Claims 3 and 17

Hattori teaches that the timing controller applies the backlight control signal of OFF state to the second direct current power conversion unit at the initial operation, and applies backlight control signal of ON state to the first direct current power conversion unit at the point that

transition into bend state of liquid crystal arranged in the LCD panel is completed when a predetermined period elapses. Hattori, col. 11, lines 16 – 20.

Claims 4 and 18

Hattori teaches that the bias voltage is a voltage of less level than the common electrode voltage. Hattori, col. 12, lines 1 – 15.

Claims 5 and 19

Hattori teaches that is -20 volt. Hattori, col. 16, line 45 – col. 18, line 31; and tables 6 – 8.

Claims 6 and 20

Hattori teaches that the timing controller outputs an alternatively selected one of the first switching signal and the second switching signal when the backlight control signal of OFF state is applied. Hattori, col. 11, lines 26 – 42; and figure 3.

Claims 29, 34, and 36

Nakamura teaches a driving method of a liquid crystal display device including a LCD module including a LCD panel, a gate driver, and a data driver; and a backlight positioned at a back side of the LCD panel. Nakamura, col. 3, line 63 – col. 4, line 24; col. 7, lines 47 – 64; and figure 1. Nakamura teaches inducing transition into bend state by a high voltage by applying a data voltage and a gate voltage not selected at initial operation of the liquid crystal display device to the LCD panel and applying an external bias voltage separately to the LCD panel. Nakamura, col. 3, lines 19 – 28; col. 4, lines 25 – 57; and figure 5. Compare Hattori, col. 4 lines 27 – 33; and col. 8, line 49 – col. 9, line 26. Nakamura teaches of interrupting the external

bias voltage when a predetermined time elapses and applying a common electrode voltage to the LCD panel. Nakamura, col. 4, lines 46 – 65; and figure 2.

Nakamura teaches a common electrode line. Nakamura, col. 3, line 67 – col. 4, line 4. Nakamura teaches that the common electrode line [common electrode] receives the bias voltage [10V-30V] at an initial operation [period t1 when the power-on reset signal is output for t1 seconds] of the LCD. Nakamura, col. 6, lines 34 – 43; and figure 7. In the embodiment shown in figure 7, the voltage is applied to both the common electrode and the storage capacitance electrode. Nakamura teaches, however, that the bias voltage may be applied exclusively to the common electrode.

> Although in this embodiment voltages are applied to both of the common electrode and the storage capacitance lines, a modification is possible in which a voltage is applied to one of those, for instance, the common electrode but no voltages are applied to the storage capacitance lines.

Nakamura, col. 7, lines 1 – 5.

Although Nakamura teaches a back light, it does not specifically teach applying a predetermined backlight driving voltage to the backlight at the same time of applying the common electrode voltage to the LCD panel.

Hattori teaches applying a predetermined backlight driving voltage to the backlight at the same time of applying the common electrode voltage to the LCD panel. Hattori, col. 4, lines 23 – 26; col. 13, lines 5 – 45; and col. 18, lines 47 – 61.

For the reasons stated in the discussion about claims 2 and 16 above, it would have been obvious to one of ordinary skill in the art at the time of the invention to combine the backlight timing controller as taught by Hattori with the liquid crystal display device as taught by

Nakamura to conserve power that would be consumed by the backlight during the start up period. See Hattori, col. 2, line 52 – col. 3, line 3.

Claims 30, 35, and 38

Nakamura teaches selecting alternatively the external bias voltage and the common electrode voltage several times and applying a selected one of the external bias voltage and the common electrode voltage to the LCD panel. Nakamura, col. 4, lines 46 – 65; and figure 2.

Claim 31

Nakamura teaches that the point that the predetermined time elapses is the point that transition into bend state is completed. Nakamura, col. 3, lines 19 – 28; col. 4, lines 25 – 46; and col. 6, lines 34 – 67.

Claim 32

Hattori teaches applying the backlight driving voltage of OFF state to the backlight upon applying the external bias voltage separately to the LCD panel. Hattori, col. 4, lines 23 – 26; col. 13, lines 5 – 45; and col. 18, lines 47 – 61.

Claim 37

Hattori teaches controlling the data voltage to be applied with a level equivalent to the level of the common electrode. Hattori, col. 12, lines 1 – 15.

Response to Arguments

5. Applicants amended the independent claims to add that the common electrode line receives the bias voltage at an initial operation of the LCD. Applicant then argued that Nakamura does not teach such.

Examiner disagrees. Nakamura teaches that the common electrode line [common electrode] receives the bias voltage [10V-30V] at an initial operation [period t1 when the power-on reset signal is output for t1 seconds] of the LCD. Nakamura, col. 6, lines 34 – 43; and figure 7. In the embodiment shown in figure 7, the voltage is applied to both the common electrode and the storage capacitance electrode. Nakamura teaches, however, that the bias voltage may be applied exclusively to the common electrode.

> Although in this embodiment voltages are applied to both of the common electrode and the storage capacitance lines, a modification is possible in which a voltage is applied to one of those, for instance, the common electrode but no voltages are applied to the storage capacitance lines.

Nakamura, col. 7, lines 1 – 5.

Conclusion

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Nonomura et al., USPN 4,411,496, teaches applying the bias voltage to the common electrode line at an initial operation of the LCD. Nonomura, col. 1, line 63 – col. 2, line 10.

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leland R. Jorgensen whose telephone number is 571-272-7768. The examiner can normally be reached on Monday through Friday, 10:00 am through 6:00 pm..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Sumati Lefkowitz can be reached on 571-272-3638. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

On July 15, 2005, the Central FAX Number will change to 571-273-8300. This new Central FAX Number is the result of relocating the Central FAX server to the Office's Alexandria, Virginia campus.

Most facsimile-transmitted patent application related correspondence is required to be sent to the Central FAX Number. To give customers time to adjust to the new Central FAX Number, faxes sent to the old number (703-872-9306) will be routed to the new number until September 15, 2005. After September 15, 2005, the old number will no longer be in service and 571-273-8300 will be the only facsimile number recognized for "centralized delivery".

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

lrj

KENT CHANG
PRIMARY EXAMINER